REMARKS

In the Office Action the Examiner rejected claims 1, 3-6, 8-19, and 21 under 35 U.S.C. 112, second paragraph, for being indefinite, claims 1 and 3-5 under 35 U.S.C. 112, first paragraph, for lacking enablement, and claims 1, 3-6, 8-19, and 21-26 under 35 U.S.C. 102 as being anticipated. Claims 2 and 7 have been withdrawn. Claims 16-26 have been canceled. Claims 1, 3-6, and 8-15 remain under examination.

With regard to claim 1 being indefinite, the Examiner pointed out that the first and second input signals and the first and second intermediate signals were not at the same logic state but claim 1 implied that they were. Claim 1 has been amended to clarify the original intent that these two pairs of signals were complementary to each other. The Examiner suggested adding term "both" to improve clarity which has been done. The Examiner further viewed the description in the claimed step of "enabling the clock inputs" as being incorrect. In this regard applicants respectfully disagree. The first and second clocked inverters are supported by transistors 222 224 for one and transistors 232 and 234 for the other. The sources of transistors 224 and 234 support the clock inputs for the two inverters. Transistor 226 functions to enable both clocked inverters when it becomes conductive. Another way of saying this is that the clock inputs of the clocked inverters are enabled when transistor 226 becomes conductive.

With regard to claim 3, the Examiner viewed the claimed operation to be incorrect. Applicants respectfully disagree. Whether the sources of transistors 224 or 226 are grounded, which is the enabled state, or floating, transistors 222 and 224 will invert a logic low input on their gates. Claim 3 has been amended to clarify the meaning. In claim 3, as now amended, the first type of logic state is supported by a logic low.

With regard to claim 16, the Examiner pointed out some potential confusion due to the claim ending with a semicolon instead of a period. Claim 16 has been canceled. Further the Examiner pointed out an inconsistent spelling in claim 26. Claim 26 has been amended to provide consistent spelling of the word.

With regard to the enablement of claims 1 and 3-5, the Examiner viewed the specification as lacking with regard to the claimed operation of the first and second input signals being at the same logic state "after providing the first and second input signals at the complementary logic states." In this regard, applicants respectfully disagree. The first and second input signals are supported by the DATA and DATAB signals in FIG. 2 and FIG. 4. This is conventional

operation of a pair of data lines or bit lines; they provide data as complementary logic states then are precharged to the same voltage. Thus, during precharge, they are both at the same logic state. Most commonly, the precharge is to a voltage that would be recognized as a logic high. The circuit of FIG. 2 is not intended to cause those conventional conditions but rather respond to them.

Further the Examiner questioned how the "enabling the clock input of the first and second inverters" achieved. As described previously, this function is supported by the functioning of transistor 226 when it becomes conductive.

With regard to anticipation of the claims, the Examiner viewed Shiratake as sufficient and further that Aoki anticipated at least the independent claims. Shiratake provides the type of operation that applicants avoid. Shiratake's circuit diagram of FIG. 15 and the corresponding timing diagram of FIG. 16 and also the circuit diagram of FIG. 24 and the corresponding timing diagram of FIG. 25 are helpful in this regard. The comparison will focus on FIGs. 24 and 25. While Q and its complement (the Q signals) are being providing as valid data signals, the OUT nodes are being held to a logic high by the clock signal Clk being a logic high. Only when the clock signal is switched to a logic low do the OUT nodes begin developing logic states that are complementary to each other. Thus, although the logic states have a correspondence to the Q signals, the OUT nodes are not responsive to a the Q signals as complementary logic states but rather are responsive to the clock signal after the logic states have become complementary. Another way of saying this is that during a first clock state, the OUT nodes are held to the same logic state by the action of transistors M8, M9, and M16. . In response to a transition from the first clock state to the second clock state and during the second clock state, nodes N1 and N2 provide complementary logic states and are latched by the action of transistors M10 and M15 and transmission gates T1 and T2 becoming conductive. Claim 1 has been amended to clarify the distinction from the operation of Shiratake. Claim 1 requires that complementary logic states be present on the first and second nodes during a first clock state and that latching be initiated in response to a transition from the first clock state to a second clock state. Thus during latching, applicants' input signals no longer need to be valid for the output signals to be valid.

Aoki provides a similar operation to that of Shiratake so that applicants' claim 1 distinguishes from Aoki on the same basis as the distinction from Shiratake.

With regard to independent claim 6, a similar distinction is present. To the extent there might be a precharge phase described in Shiratake, it is not one in which entering it causes the input signals to become the same logic state and the latch comprised of clocked inverters is enabled. Dependent claims 8 and 9 also distinguish from the cited art.

With regard to independent claim 10, which has been amended for clarification, the operation described for the clocked inverters distinguishes from that for either Shiratake or Aoki in a manner similar to that described for claim 1. Dependent claims 11-15 also distinguish from Shiratake and Aoki.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning the current application.

Respectfully submitted,

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